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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/875,673	06/05/2001	Sailesh Kottapalli	42390P11313	7551

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EXAMINER
CHOI, WOO H

ART UNIT	PAPER NUMBER
2189	

Leo V. Novakoski
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/875,673	KOTTAPALLI, SAILESH	
	Examiner	Art Unit	
	Woo H. Choi	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 18-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,18-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

S.O.-D.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 2 – 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 2 recites the limitation "the first and second entries correspond to an entry to which a portion of the target address maps and an adjacent entry, respectively." There two arrays where entries can be found, a data array and a tag array. It is not clear which of the two arrays 'an entry' and 'an adjacent entry' are claimed to be in.

For the purposes of this examination, 'an entry' and 'an adjacent' entry' will be treated as entries in either of the two arrays.

4. Claims 3 – 5 are rejected for including the deficiency of their parent claims.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 – 5, 9, 11 – 12, 14 – 16, and 18 – 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Cohen *et al.* (US Patent No. 5,784,590, hereinafter "Cohen").

7. With respect to claims 1 and 9, Cohen discloses an apparatus (figure 1) comprising:

a tag array to store address information for data blocks (figure 1, 26, figure 2, 74, 2KB slave cache has an array or 64 tags 60s and slave data valid bits 80 – 83) ;

a data array to store data blocks (figure 1, 26, figure 2, 74, 2KB slave cache has an array of 64 data blocks 50 – 53);

a decoder to access first and second entries of the tag array responsive to a request; and

hit/miss logic to process the request, responsive to hit/miss signals triggered by the access to the first and second entries (col. 7, lines 26 – 33, the cache design requires access to all tag entries, including first and second entries, for comparison to determine hit/miss. If all entries miss, the slave cache misses, whereas if one entry hits and the others miss the slave cache hits),

wherein a first set index (figure 4, slave cache index A21 – A26) is derived from set bits (col. 3, lines 9 – 10) and a second set index (master cache index that includes A20 – A26) is derived from the first set index (figure 4, and col. 8, lines 4 – 16, master cache index can be formed by adding A20 from the tag field of the slave cache). The Examiner also notes that as currently stated, the wherein clause is not related in any way to the rest of the body of the claim.

8. With respect to claim 2, the data blocks are instruction blocks (figure 1, 26), the request specifies a target address for an instruction block, and the first and second entries correspond to an entry to which a portion of the target address maps (figure 4, and lines 37 – 45, tag entry contains a portion of the target address) and an adjacent entry (all entries in an array are adjacent entries, since each entry in an array is next to at least one other entry), respectively.

9. With respect to claims 3 and 11, the hit/miss logic triggers a request to a higher-level cache if the access to the first entry of the tag array misses (col. 7, lines 26 – 33).

10. With respect to claim 4, the hit/miss logic signals the higher-level cache (figure 1, 30, Master Cache) to return a full cache line if the accesses to the first and second entries both miss (figure 7, col. 10, line 35 – col. 12, line 9. A slave cache tag miss, i.e. all entries including first and second entries miss, causes the slave valid bits to be set to zero, step 102, which means that all four sub-lines or full cache line is being requested. See also col. 11 lines 7 – 10).

11. With respect to claim 5, the hit/miss logic signals the higher-level cache to return a partial cache line if the access to the first entry misses and the access to the second entry hits (figure 7, col. 10, line 35 – col. 12, line 9. A slave cache tag hit, i.e. one entry or a second entry hits and all the other entries including a first entry miss, then valid bits for sub-lines that are valid in the slave cache are sent to the master, step 106, then the master consolidates this request with other

requests that are in the pipeline for the same cache line, steps 114 – 126, and the resulting partial cache line, i.e. sub-lines that are not valid, is sent to the slave, step 128).

12. With respect to claim 12, see rejections of claims 4 and 5.

13. With respect to claims 14 and 16, Cohen discloses a device comprising:

a first cache (figure 1, 26) including a plurality of entries, each entry to store an instruction block having a first size (figure 2, 2KB slave cache store instruction blocks of 8 bytes);

a decoder to generate multiple look-ups to the first cache responsive to a target address (col. 7, lines 26 – 33, the cache design requires that all tag entries be looked-up for comparison to determine hit/miss. See also figure 7, steps 104, 116 and 118. Steps 116 and 118 indeces and tags are looked-up to determine whether there is another request, i.e. look-ups, to the same target address to consolidate the slave cache valid bits and the requested sub-lines);

a second cache including a plurality of entries (figure 2, 32KB Master has 128 entries), each entry to store an instruction block having a second size (32 bytes) that is greater than the first size; and

a request manager to transfer to the first cache an instruction block from the second cache having one of a plurality of sizes, responsive to results of the primary (figure 7, step 104) and secondary (figure 7, steps 116 and 118) look-ups (figure 7, see discussions of this figure in rejections of claims 4 and 5 above. Size of the transferred instruction block depends on the look-ups in steps 104, 116, and 118),

wherein a first set index (figure 4, slave cache index A21 – A26) is derived from set bits (col. 3, lines 9 – 10) and a second set index (master cache index that includes A20 – A26) is derived from the first set index (figure 4, and col. 8, lines 4 – 16, master cache index can be formed by adding A20 from the tag field of the slave cache).

14. With respect to claim 15, the multiple look-ups are primary and secondary look-ups (see discussion of claim 14 above) and the request manager transfers an instruction block having the second size responsive to the primary and secondary look-ups missing in the first cache (as discussed above, size of the transferred block varies depending on the results of various look-ups and resulting consolidations with the full cache line of the master cache being transferred if all of the look-ups miss).

15. With respect to claim 18, all of the multiple look-ups are processed if the target address meets a first criterion (all entries in the slave cache are processed regardless of what the target address is, therefore, they are all processed if the target address meets a first criterion).

16. With respect to claim 19, the first criterion is that the target address maps to a boundary of the instruction block of the second cache (as discussed above, all entries in the slave cache are processed regardless of what the criterion is).

17. With respect to claim 20, all of the multiple look-ups (steps 104 and 108) are processed if the target address meets a first criterion (figure 7, step 116, index match, look-ups in steps 104,

118 are processed if the result of the index match in step 116 is yes), and only a first of the multiple look-ups is processed if the target address does not meet the first criterion (only step 104 is processed if there is no index match).

18. With respect to claims 21 and 22, the multiple look-ups comprise primary and secondary look-ups (figure 7, steps 104 and 118) and the first cache includes a standard port, that comprises a tag port and a data port, to process the primary look-up and a pseudo-port, that comprises a tag port, to process the secondary look-up (look-up in step 104 is a standard look-up through a regular tag port, the secondary look-up is not through a real tag port but a tag look-up in the request pipeline for the same target address).

19. With respect to claim 23, the decoder drives a first index (figure 4) on the standard port and a second index (figure 8A, index into the pipeline or pipeline stage), derived from the first index, on the pseudo port.

20. With respect to claim 24, Cohen discloses a computer system comprising:

a thread control unit to schedule execution of instructions from multiple threads (col. 7, lines 43 – 53, multiple execution pipelines suggest multi-threaded execution of instructions);

an execution module to execute the scheduled instructions (execution module is a necessary component of a super-scalar CPU); and

a memory hierarchy to supply the execution module with instructions for the multiple threads, the memory hierarchy including:

a first cache to store instruction in multiple cache lines of a first size (figure 1, 26, slave cache line consists of 8 byte blocks);

a second cache to store instructions in multiple cache lines of a second size that is different from the first size (figure 1, 30, and figure 2, master cache line consists of 32 byte line data);

a main memory (figure 1, 34); and

to a cache controller to generate multiple look-ups to the first cache responsive to an instruction address and to transfer a block of instructions to the first cache responsive to hit/miss signals generated by the multiple look-ups (figure 7, all entries in the slave cache need to be looked-up to determine cache hit/miss, see discussions of figure 7 above).

21. With respect to claim 25, see rejections of claims 4 and 5.

22. With respect to claim 26, the system further comprises a memory controller, wherein the memory controller transfers instructions from the main memory responsive to a miss in a second cache controller (col. 5, lines 11 – 14).

23. Claims 1 – 4 and 6 – 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Witt (US Patent No. 5,623,627).

24. With respect to claims 1 and 9, Witt discloses an apparatus (figure 2) comprising:

a tag array to store address information for data blocks (figure 2, 182 and 390);

a data array to store data blocks (180);

a decoder to access first (figure 3A, step 515)and second (figure 3A, step 525) entries of the tag array responsive to a request (see also figure 6, multiple look-ups are generated in the linear tag array as well); and

hit/miss logic to process the request, responsive to hit/miss signals triggered by the access to the first and second entries (figure 3A),

wherein a first set index (figure 5, PTAG index) is derived from set bits (index 11 – 4 of the address 31) and a second index (figure 14A) is derived from the first set index (col. 16, lines 63 – col. 17, line 7, tag, index, and offset values from the first level cache miss is used to access replacement cache 60 of figure 2).

25. With respect to claim 2, the data blocks are instruction blocks (figure 3, 180), the request specifies a target address for an instruction block, and the first and second entries correspond to an entry to which a portion of the target address maps and an adjacent entry (all entries in an array are adjacent entries, since each entry in an array is next to at least one other entry), respectively.

26. With respect to claims 3 and 11, the hit/miss logic triggers a request to a higher-level cache (figure 2, 60) if the access to the first entry of the tag array misses (figure 3A, steps 515 – 560).

27. With respect to claim 4, the hit/miss logic signals the higher-level cache to return a full cache line if the accesses to the first and second entries both miss (figure 3A, steps 515 – 560).

28. With respect to claim 6, the tag array includes first (figure 2, linear inst. tag array port) and second (figure 2, physical inst. tag array port) tag ports to process the first and second accesses.

29. With respect to claim 7, the data array includes a first data port to process a first access that hits in the tag array, the first tag and data arrays forming a standard port (figure 2, the linear tag array and the first level instruction store forms a standard first level cache with a standard port).

30. With respect to claims 8 and 10, the decoder drives a first index to the first tag port and drives a modified version of the first index to the second tag port (figures 5, 8 and 12).

32. Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by Kranich (US Patent No. 5,752,263).

Kranich discloses a method comprising:

detecting a target address (col. 4, lines 37 – 41);

generating first (figure 2, 90) and second (110) look-ups to a cache responsive to a target address comprising:

generating a standard look-up to a first set determined from a portion of the target address (the first look-up 90 is a standard look-up); and

generating a pseudo-look-up to second set adjacent to the first set (the second look-up is a pseudo look-up to determine whether the adjacent cache line is to be prefetched) and.

retrieving a data block from a second cache (40 or 18) responsive to hit/miss signals generated by the first and second look-ups, wherein a first set index is derived from set bits (col. 4, lines 37 – 45, index into tag array is derived from the target address that has address bits set to 0 or 1) and a second set index is derived from the first set index (figure 3, 150 and 156, see also col. 7, lines 1 – 3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Woo H. Choi
June 9, 2005